REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 15-32 are presently active; Claims 1-14 were previously canceled without prejudice. Claims 15, 20, and 21 have been presently amended. No new matter has been added.

In the outstanding Office Action, Claims 15-19, 25, 27, and 28 were rejected under 35 U.S.C. § 102(b) as being anticipated by <u>Sakamoto et al</u> (U.S. Pat. No. 5,286,983). Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over <u>Sakamoto et al</u>. Claims 20-24 and 29-32 were objected to for being dependent from a rejected base claim but would be allowable if rewritten in independent form to include the limitations of the base claim and any intervening claims.

Applicants acknowledge with appreciation the indication of allowable subject matter in Claims 20-24 and 29-32. In an effort to expedite prosecution of this application, a part of the subject matter of Claim 20 has been included in Claim 15. This feature (i.e., a channel level of the transistors is situated between a level of the storage capacitor bus and that of the row selection lines forming gate of the transistors) is a features not shown in <u>Sakamoto et al</u>.

For instance, the Office Action associates in <u>Sakamoto et al</u> element 32 with a row selection line. In <u>Sakamoto et al</u>'s Figure 8, it is clear that the channel level of the transistor (i.e., element 54) is on the surface of the transparent substrate 48. In <u>Sakamoto et al</u>'s Figure 9B, it is clear that element 32a (which under the Office's interpretation would be a part of the row selection line is also on the surface of the transparent substrate 48. Therefore, <u>Sakamoto et al</u> do not disclose a channel level of a transistor situated between a level of the storage capacitor bus and that of the row selection lines forming gate of the transistors.

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Thus, since M.P.E.P. § 2131 requires for anticipation that each and every feature of

Claims 15 and dependent Claims 16-32 are not anticipated by <u>Sakamoto et al</u>, and should be

the claimed invention must be shown in as complete detail as is contained in the claim,

passed to allowance.

Consequently, in view of the present amendment and in light of the above

discussions, the outstanding grounds for rejection are believed to have been overcome. The

application as amended herewith is believed to be in condition for formal allowance. An

early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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